Characteristics of Near-field Magnetic Radiated Emissions from VLSI Microcontroller Devices

James P. Muccioli — JASTECH
Mike Catherwood, Dale Stevens — MOTOROLA

EMC TEST & DESIGN, NOVEMBER 1993 ©

Abstract

This article discusses the characteristics of near-field radiated magnetic emissions from the Motorola MC68HC05 family of HCMOS VLSI microcontrollers. The relationships between shrink level, internal signal rise/fall times, and emission levels will be examined. Device shrinking and its effect on the emission profile will be explained.

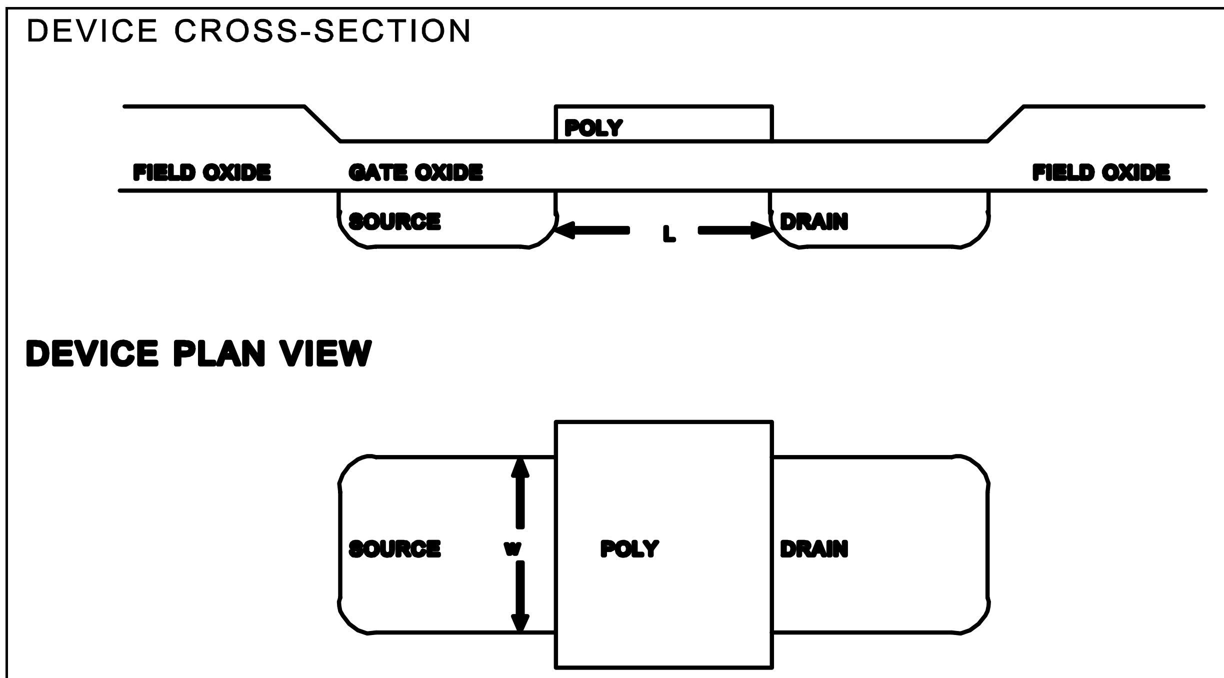
The correspondence between application and integrated circuit (IC) level EMI reduction techniques will be demonstrated by examining the influence of certain IC level system and circuit design techniques on the emission profile of various experimental devices.

Integrated Circuit Process Background

VLSI semiconductor manufacturers often refer to a device as having been "shrunk" from a predetermined "drawn" size. For the Motorola products discussed in this paper, the "drawn" size refers to the minimum MOS device effective gate poly-silicon (often abbreviated to "poly") length used within the device when it is designed. Figure 1 shows the layout of a MOS transistor and its critical dimensions. For the devices discussed in this article, the drawn size is 3 microns ($3x10^{-6}$ metre). A device which is manufactured at 60% shrink will therefore have an effective gate poly length of approximately (1-0.6) x $3x10^{-6}$ = 1.2 microns on the die itself. Similarly, 50% shrink product will have an effective gate poly length of approximately 1.5 microns. Because different manufacturers use different methods of representing drawn sizes (e.g. minimum line width) and also different drawn dimensions, comparing what are referred to as 50% shrink products may not always be an apples to apples comparison. In addition, differing processing techniques will also affect the actual physical dimensions on the device.

There are many advantages to shrinking devices, so VLSI IC manufacturers will generally continue to do so as fast as the technology (or robustness of the design) allows. Obvious benefits include more dies per wafer (dpw) and better yields (even if the defect density remains the same, there will be less defects per die). Other benefits come from the electrical effects associated with shrinking. As a MOS transistor is shrunk, it tends to become faster (less propagation delay). If the gate oxide thickness is also scaled, the gate capacitance and device saturation current (drive capability) will both increase by roughly the same amount related to the lateral (thickness) shrink factor. The interconnect capacitance (the transistor load) decreases by roughly the square of the shrink factor. From an RF emissions point of view, some of these factors work against each other, however, the overall effect of shrinking has been shown to increase device operating speed and RF emissions. It is interesting to note, however, that pin output buffers are usually resized to maintain the same or similar electrical characteristics between the old device and its new shrunk counterpart. For single-chip devices (i.e. no external address/data/control buses) such as those examined in this article, this usually makes little

difference due to the relatively infrequent (software driven) output port transitions. However, the effect of resizing output buffers on an expanded bus device can be noticeable and will form the basis of a future article. The observations in this article can therefore be applied only to single-chip devices which do not use any high speed peripheral output functions (e.g. a fast synchronous serial port).



When a CMOS buffer changes state, the P-channel and N-channel devices do not switch exclusively. Depending upon the transition speed of the input signal, there is a portion of time during the transition when both devices will be conducting. The resultant (characteristically CMOS) Idd current spike is referred to as simultaneous, shoot-through or cross-over current. A positive attribute of the faster internal rise and fall times associated with a shrunk device is that the width of any simultaneous current will be shorter, reducing total Idd. However, the resultant transition time of that Idd pulse will also be faster, which from the traditional definition of signal band-width ($f1 = 1/\Pi\ t_r$), will have a negative effect on RF emissions.

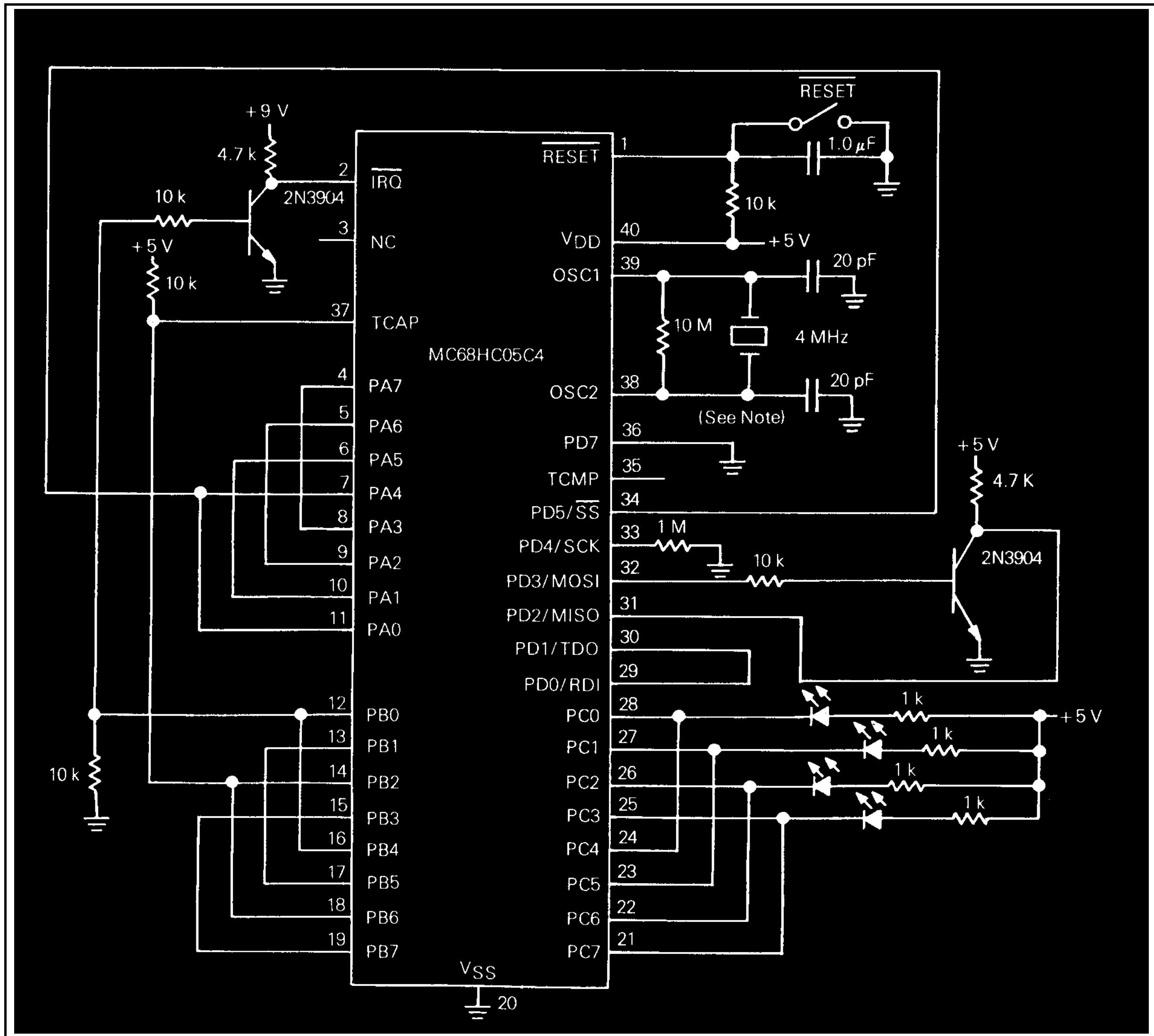
In single-chip microcontrollers such as those examined in this article, the Idd signal in the supply loop contributes most of the energy responsible for the RF emissions from the device. Although the Idd amplitude decreases for higher shrink devices, the increased bandwidth of the Idd signal resulting from the faster Idd transition time has been observed to dominate the RF emission signature. In the absence of any design modifications, it is generally true to say that the higher the shrink level, the broader the expected bandwidth of RF emissions. The broader bandwidth spectrum is typically dominated by harmonics of the oscillator and internal clocks of the MCU, which appear above a floor of asynchronous emissions. Consequently, most emission problems can be attributed to the amplitude of these clock harmonics. Therefore, techniques to reduce the radiating loop area or the clock current passing through it have been shown to significantly improve the EMC performance of a device in many applications.

Bringing supply pins closer together and onto package pins with shorter leadframe fingers reduces radiating loop area. Reducing the size of large clock buffers will make the devices weaker, reducing the magnitude and edge speed of any simultaneous current which will consequently reduce the clock current harmonic amplitude and bandwidth. Carefully sizing other large switching devices which switch aperiodically (e.g. those related to address and data bus function) will benefit the emission spectrum by reducing the amplitude of the asynchronous emission floor. In some narrowband applications, this can be more critical than reducing clock harmonics.

Integrated Circuit Test Configurations

The device examined in this article is the Motorola MC68HC05C4 single chip microcontroller. It features 4K bytes of ROM, 176 bytes of RAM, a 16-bit timer, an SPI (Serial Peripheral Interface) and an SCI (UART). This MCU was chosen because it has been in production for many years and has had a long history of production shrinks. In addition, the device has also been used in an RF emission reduction program which has provided a number of interesting experimental versions. This article examines 35%, 42%, 50%, and 60% shrink silicon plus two experimental 50% lots (a low-noise 50% shrink and a special oxide layer with 50% shrink). RF emission reduction techniques which are not directly related to the silicon design, such as those discussed later in this article, are excluded in order to provide fair comparisons of emission spectra. Although the more recent M68HC05 family members do make use of techniques like supply loop area reduction to reduce RF emissions, they do not offer the wide range of shrink levels available from the older device.

Nearly all ROM versions of the M68HC05 family feature a self-check mode of operation. These devices can be forced into this mode out of reset, after which they will execute Motorola test code from a small dedicated ROM area (typically 240 bytes). The self-check configuration is shown in Figure 2. Self-check is designed to provide a gross functional test of a device by continuously cycling through several test routines. Each routine drives Port C to a predefined state. The self-check code enters a tight infinite loop when the first failure is detected, freezing Port C which is typically connected to some LEDs to indicate test status. When self-check is running successfully, the LEDs will flash periodically. Although fault coverage is fairly low, self-check does exercise a large portion of the device and is therefore a useful tool for providing relative RF emission measurements.



Test Methodology

The magnetic field generated by an integrated circuit can be measured in a controlled manner that yields repeatable results. This magnetic field is related to the electromagnetic radiation potential of the integrated circuit and of the electronic module of which it is a part. The test method used in this article for evaluating the near field magnetic component of the electromagnetic radiation from an integrated circuit uses a square loop probe. The square loop probe[1] is 1 cm in size to optimize the measured narrowband magnetic RF emissions from 1 MHz to 1000 MHz at a controlled distance and orientation from an integrated circuit. The probe can be used in a non-shielded room since the magnetic fields related to the electromagnetic radiation potential of the integrated circuit affect the probe and it is relatively insensitive to stray electric fields.

[1] SAE IC-EMC task force draft document, "Integrated Circuit Radiated Emissions Procedure from 1 MHz to 1000 MHz, Magnetic Field-loop probe," January 1993.

The surface of the integrated circuit is mapped by orienting the probe for maximum sensitivity and then repeating the measurement after moving the probe to the next location. The square loop probe can be calibrated in a Transverse Electromagnetic Mode (TEM) cell and has a typical voltage output shown in Table 2 when exposed to an E-field of one volt/meter and a magnetic field intensity of .0027 amperes/meter from 10 MHz to 1100 MHz.

FREQUENCY MHz	SQUARE LOOP PROBE mV
10	0.02
50	0.18
100	0.34
200	0.55
300	0.66
400	0.73
500	0.86
600	0.94
700	1.10
800	1.14
900	1.16
1000	1.29
1100	0.97

Table 1. Square loop probe cablibation data (Courtesy of Fischer Custom Communications).

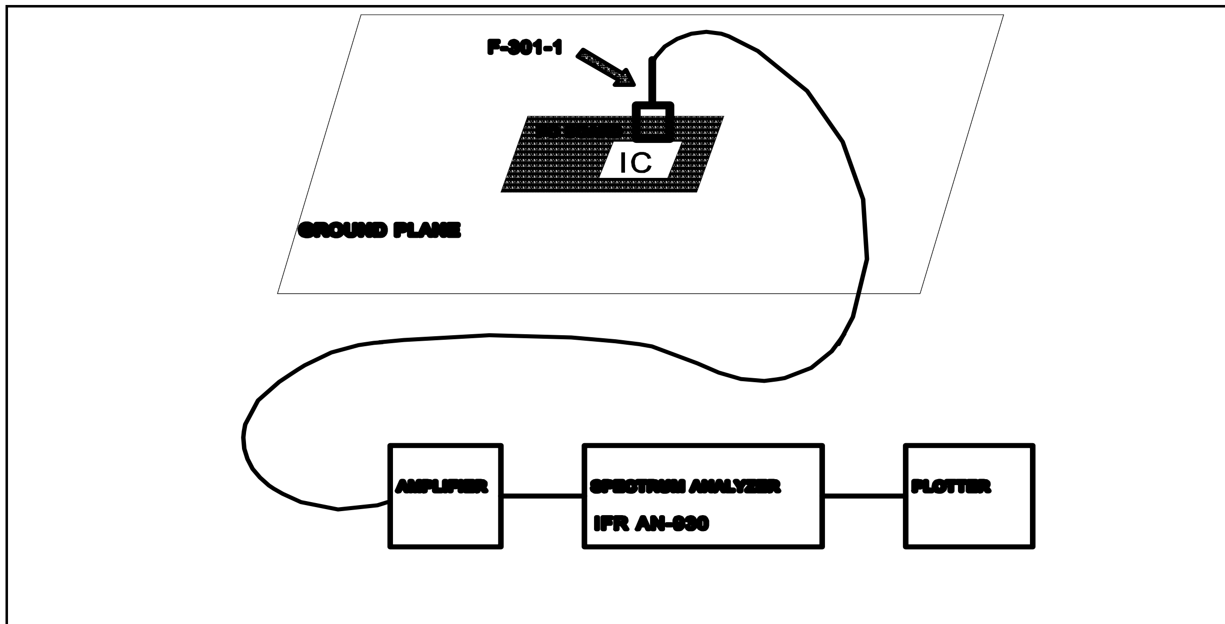
The square loop probe (F-301-1)[2] is in series with a 20 db pre-amplifier (Mini-Circuits ZFL-1000LN)[3] and is connected to a spectrum analyzer (IFR AN-930)[4] as shown in Figures 3 and 4. The system gain of the measuring equipment should be known with an accuracy of +/- 0.5 db. If the signals being measured by the square loop probe are within 6 db of the system noise floor, then a smaller resolution bandwidth should be used on the spectrum analyzer. The first measurement taken in each frequency band of the spectrum analyzer should be the ambient system level to assure that any ambient signals present are at least 6 db below the signals of the integrated circuit. This is accomplished by taking the ambient measurement with the square loop probe placed at a fixed distance on top of the integrated circuit in the measurement position with no power applied to device under test. The device under test should then be

[2]FCC F-301-1 Probe, Fischer Custom Communications Inc., 3121 West 139th Street, Unit F, Hawthorne, California 90250, Phone 310/644-0728.

[3]Mini-Circuits ZFL-1000LN, Mini-Circuits™, P.O. Box 350166, Brooklyn, New York 11235-0003, Phone 718/934-4500.

[4]IFR AN-930, IFR Systems, Inc., 10200 West York Street, Wichita, Kansas 67215-8935, Phone 316/522-4981.

energized and a complete operational check of the integrated circuit test code should be performed to assure proper functioning of the device.



Test Results

Internal transition times were measured by microprobing an internal primary clock driver buffer on each of the four standard shrinks and on the noise reduced 50% shrink device. Measuring external (pin) transition times is less meaningful, as the output buffers are generally resized when a device is shrunk in order to maintain consistency of electrical characteristics between successive shrinks. The results are shown in Table 2 and correspond with the radiated emission spectra and theoretical

expectations, indicating that, if unmodified, the higher shrink devices have faster internal transition times.

Shrink	t_r	t_f
35%	6.9 nS	7.3 nS
42%	5.4 nS	6.5 nS
50%	3.8 nS	5.5 nS
50% (low-noise)	8.6 nS	6.6 nS
60%	3.8 nS	4.7 nS

Table 2. Internal clock transition measurements.

Figure 5 shows the system noise floor with the pre-amplifier and the F-301-1 square loop probe. The system noise floor from 1 MHz to 400 MHz is below -100 dbm when the 20 db gain is factored into the spectrum analyzer.

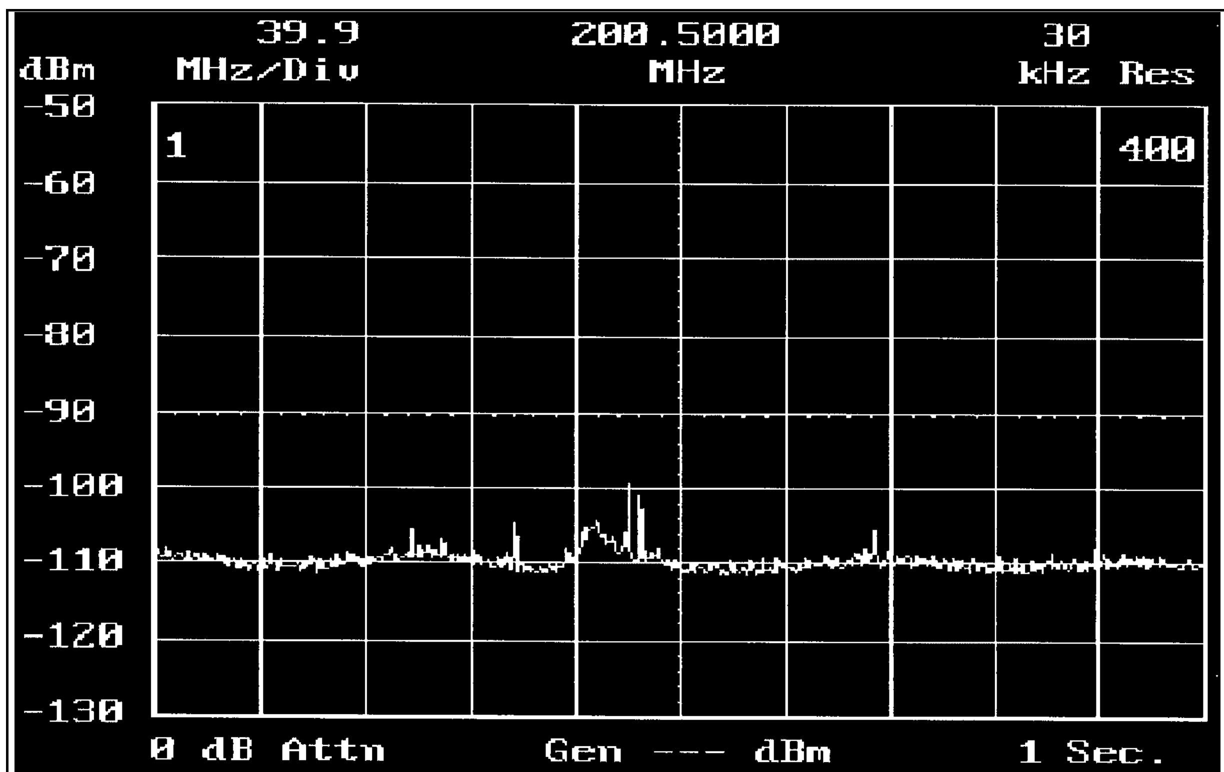


Figure 6 shows the measured magnetic emissions of an eight bit microprocessor with a 1.9 micron process size.

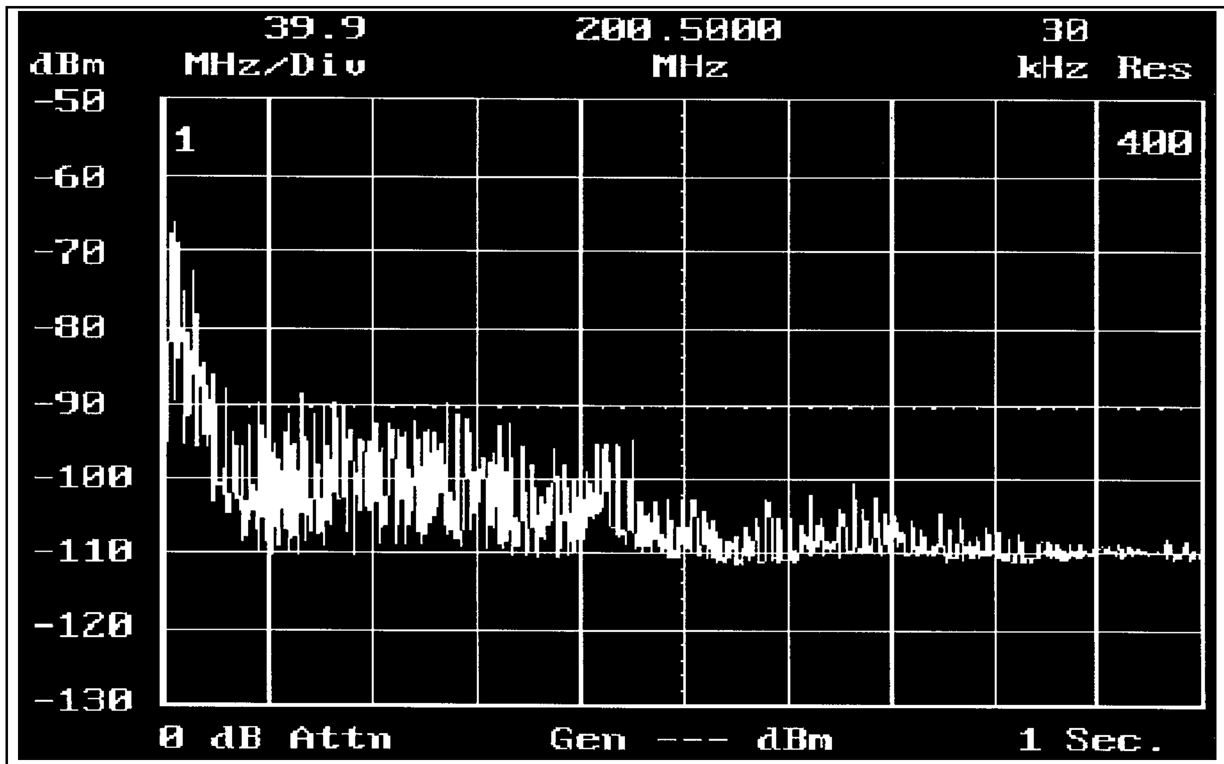
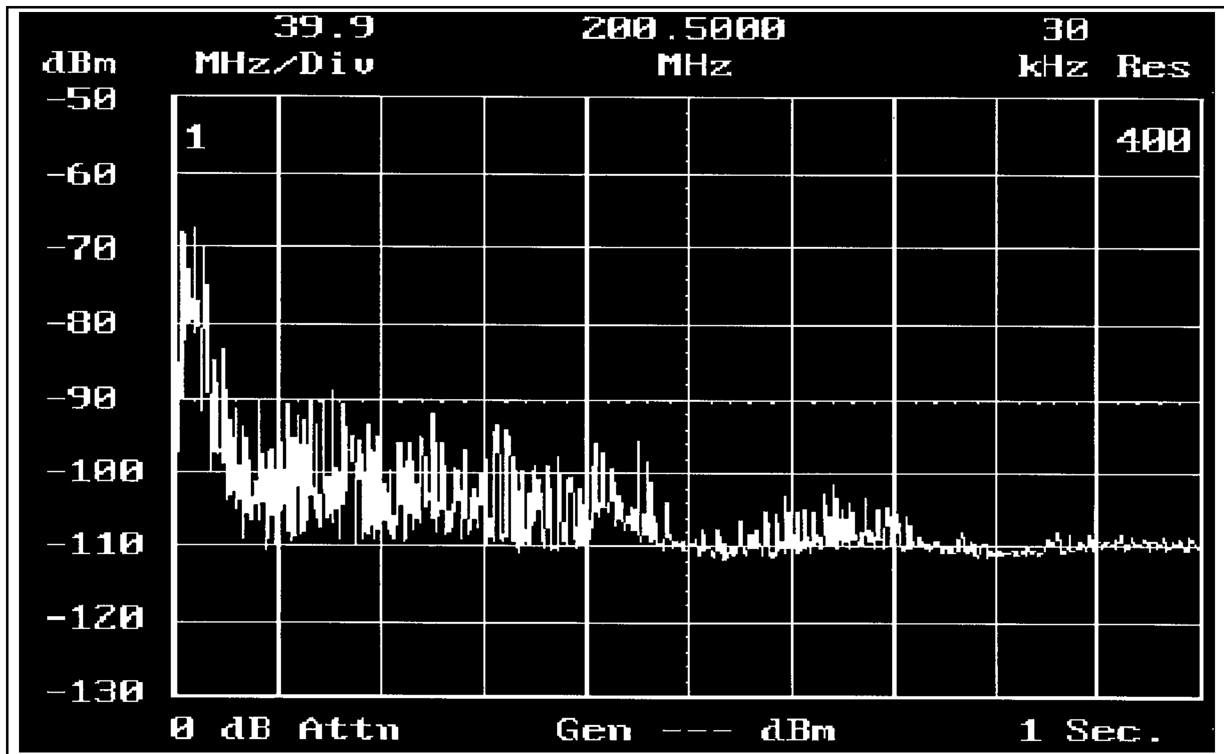


Figure 7 shows the measured magnetic emissions of an eight bit microprocessor with a



1.7 micron process size.

Figure 8 shows the measured magnetic emissions of an eight bit microprocessor with a 1.5 micron process size.

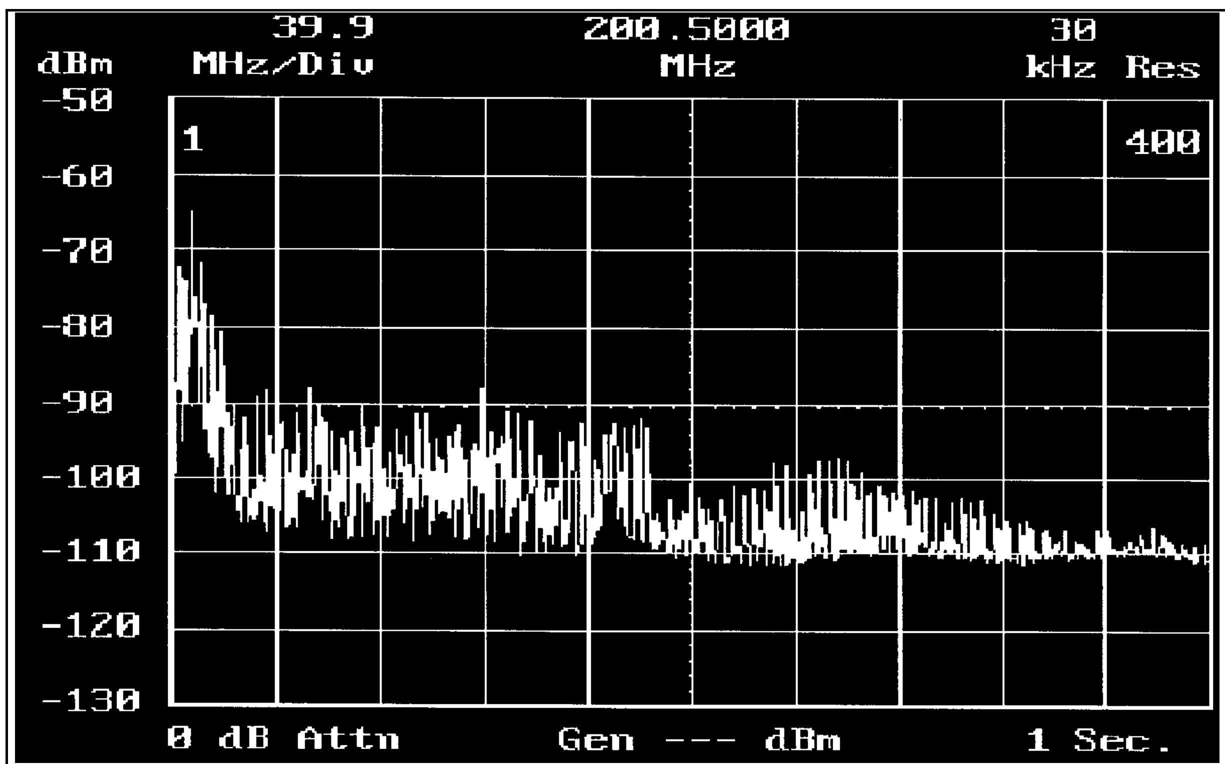
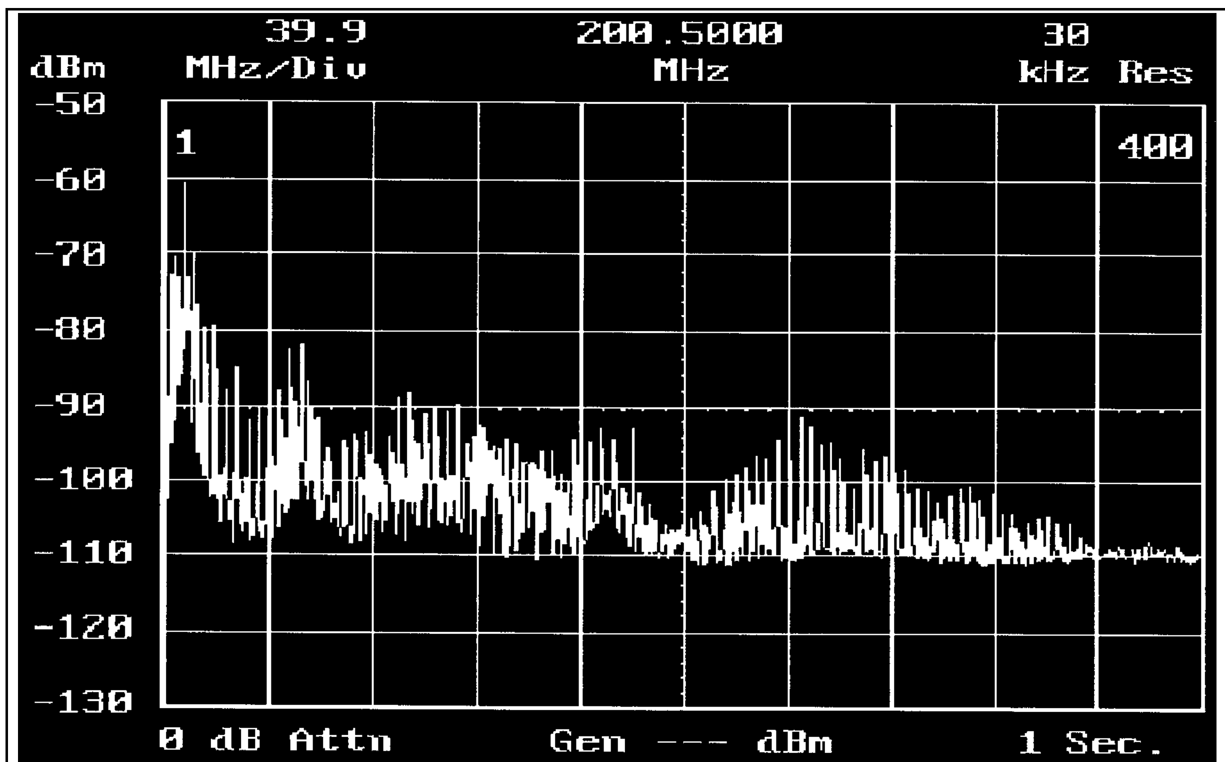


Figure 9 shows the measured magnetic emissions of an eight bit microprocessor with a



1.2 micron process size.

Figure 10 shows the measured magnetic emissions of an eight bit microprocessor with a low noise 1.5 micron process size.

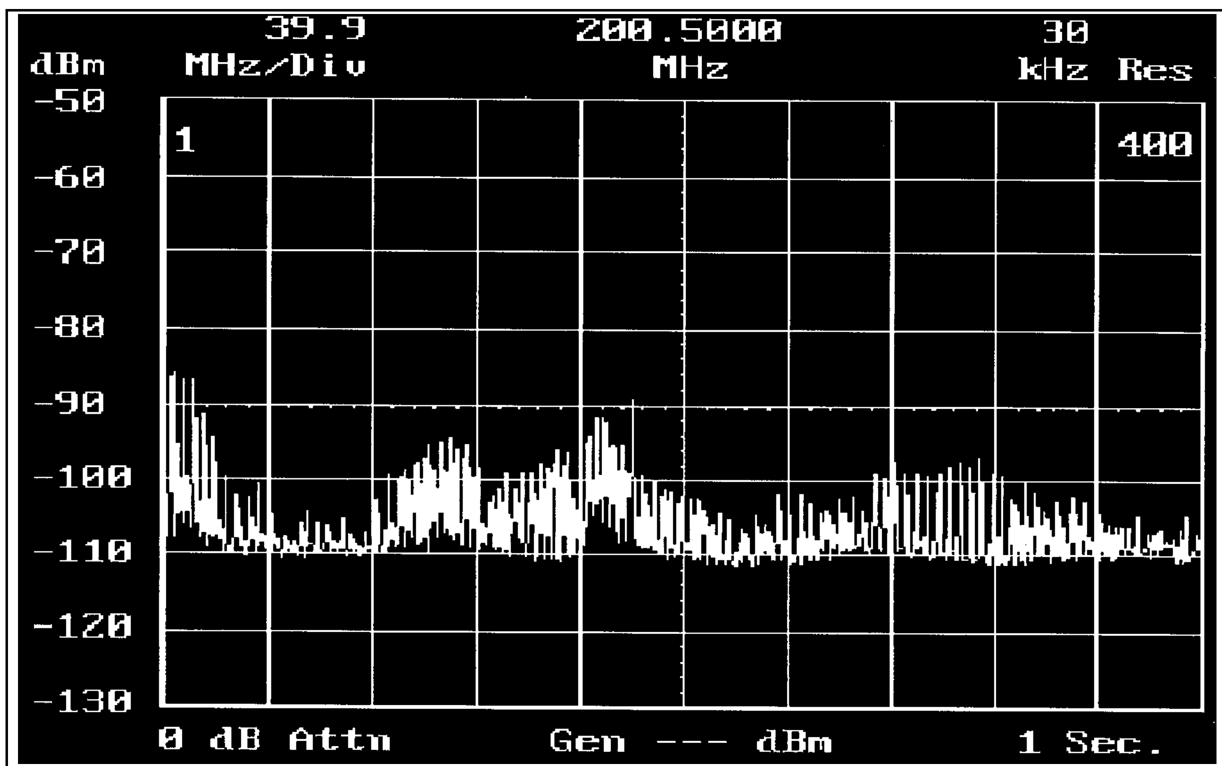
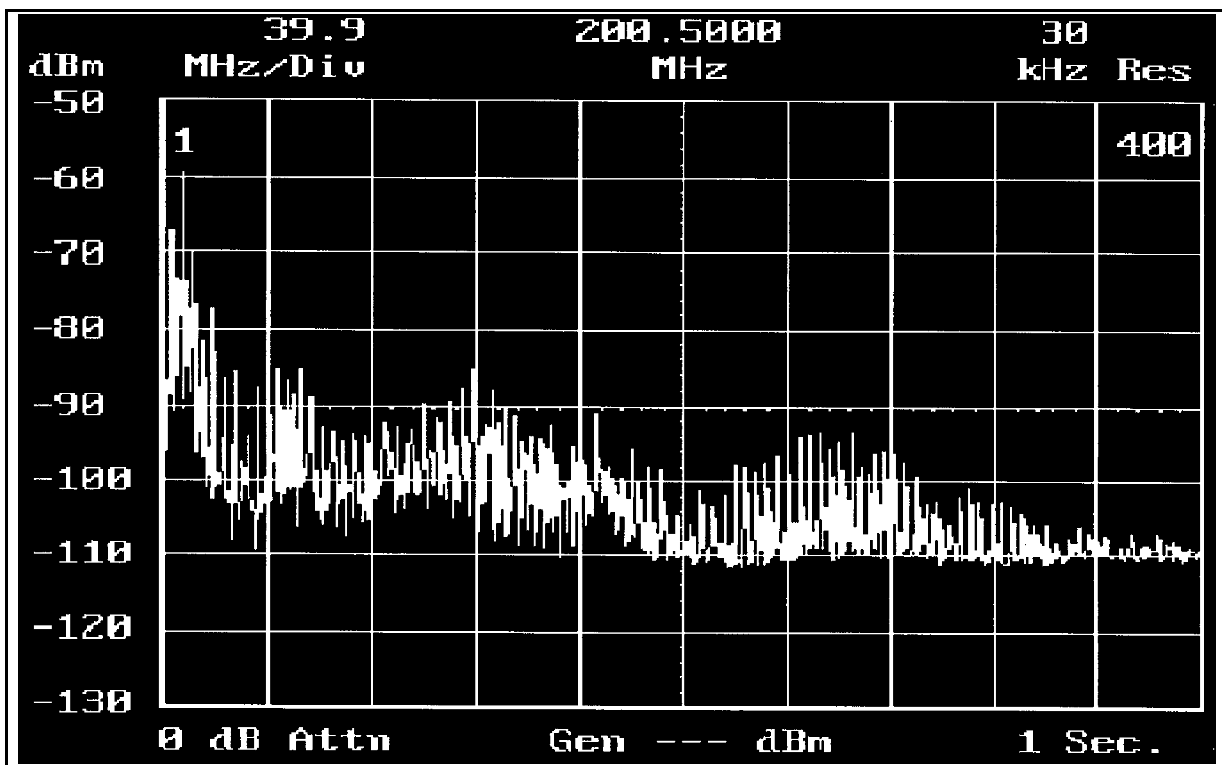


Figure 11 shows the measured magnetic emissions of an eight bit microprocessor with



experimental 1.5 micron process size.

Analysis of data

The "signatures" or general shapes of the spectra of the devices tested are all much the same, as is to be expected for devices of the same basic topology and function. The difference in radiated emissions between the 35% and 42% devices is small. The 42%

device spectrum actually appears to have a slightly lower bandwidth than that of the 35% device. However, at this point (about 300 MHz), the amplitude of both spectra is approaching the noise floor of the measurement, which makes accurate assessment of the actual bandwidth difficult.

The emissions bandwidth between the 42%, 50%, and 60% products shows a consistent increasing trend. This trend reflects increasing clock speeds and correlates with the microprober observations shown in Table 2.

The emission spectral amplitude also increases with each shrink, with most of the increase occurring between 200 MHz and 450 MHz. However, the incremental increase in harmonic amplitude between the 42% and 50% shrinks is noticeably greater than that between any of the other shrink iterations. In order to try and identify the mechanism behind this increase, a 50% shrink experimental device was processed with the gate oxide thickness increased to that of the 42% device. This had the effect of reducing only the gate capacitance, as the field oxide and all other dimensions remained constant. Reducing the gate capacitance also had the secondary effect of reducing the transistor saturation current, all else being equal.

The spectrum of this device is shown in Figure 11 and is remarkably similar to that of the 60% device. Since, the main difference between the 42% standard and 50% experimental devices is a reduction in interconnect capacitance, it is reasonable to surmise that additional lateral (gate oxide) shrink will significantly reduce the RF emissions. We can therefore conclude that, at least for the higher shrink levels, the gate capacitance has a significant influence on the overall emission spectrum. Further experiments with still thinner oxides are planned.

In addition to the oxide experiment, a noise reduction experiment was performed using production processing for a 50% shrink device which had several circuit changes implemented to try and moderate internal transition times. The Vdd/Vss pin-out of the noise reduced device was not changed to show correlation to standard devices.   The spectrum of this device is shown in Figure 10. The changes reduce the amplitude of the harmonics below about 200 MHz by more than 10 db but have little effect on the bandwidth, which remains about the same as that of the regular 50% device. The large clock driver measured with the microprober confirms the effect of the resizing and probably accounts for much of the emission improvement. However, not all clock buffers were modified in the resizing of the device, which may explain the continuing presence of the higher frequency components.

ACKNOWLEDGEMENTS

The authors wish to thank Mr. Joseph Fischer and Mrs. Sandra Muccioli for their assistance in helping prepare this paper.

REFERENCE

Catherwood, Mike "HCMOS VLSI Design For EMC," EMC/ESD International

Conference Proceeding, April 1992.

Muccioli, James P. "IC PROCESS SIZE EFFECTS ON EMC," EMC Test & Design, June 1993.

Muccioli, James P. "Radiated Emissions of Very Large Scale Integrated Circuits," IEEE International Symposium on Electromagnetic Compatibility, August 1990.